

GeForce6100SM-M2

REV: 1.0

PCB:15-V09-011010

BOM:81-605-V09110

MCP68S Real S3

Components :718PCS

MCP61S Real S3

Components :693PCS

Add R26.R28.R29.R30

Del R48

Page Index

01-COVER PAGE

02-BLOCK DIAGRAM

03-BLOCK DISTRIBUTION

04-CPU M2-1 HyperTransport

05-CPU M2-1 DDR2

06-CPU M2-3 Miscellany

07-CPU M2-4 Power and Ground

08-DDR2 DIMM

09-DDR2 Termination

10-MCP61 HT

11-MCP61 PCI-E X16

12-MCP61 PCI-E X1/RGMII/DAC

13-MCP61 PCI

14-MCP61 SATA/IDE

15-MCP61 AUDIO/USB/MISC

16-MCP61 PWR/GND

17-MCP61 DECOUPLING

18-VGA

19-PCI-E X16 CONN

20-PCI1/PCI2

21-PCI-E X1 / AC131 / SPI

22-LPC SIO-ITE8726F/FDD

23-PS2/COM/LPT

24-USB / Lan Conn.

25-AUDIO ALC861/660/662

26-AUDIO ALC861/660/662(PANEL)

27-PWR CON/FNT PNL

28-CPU VCORE

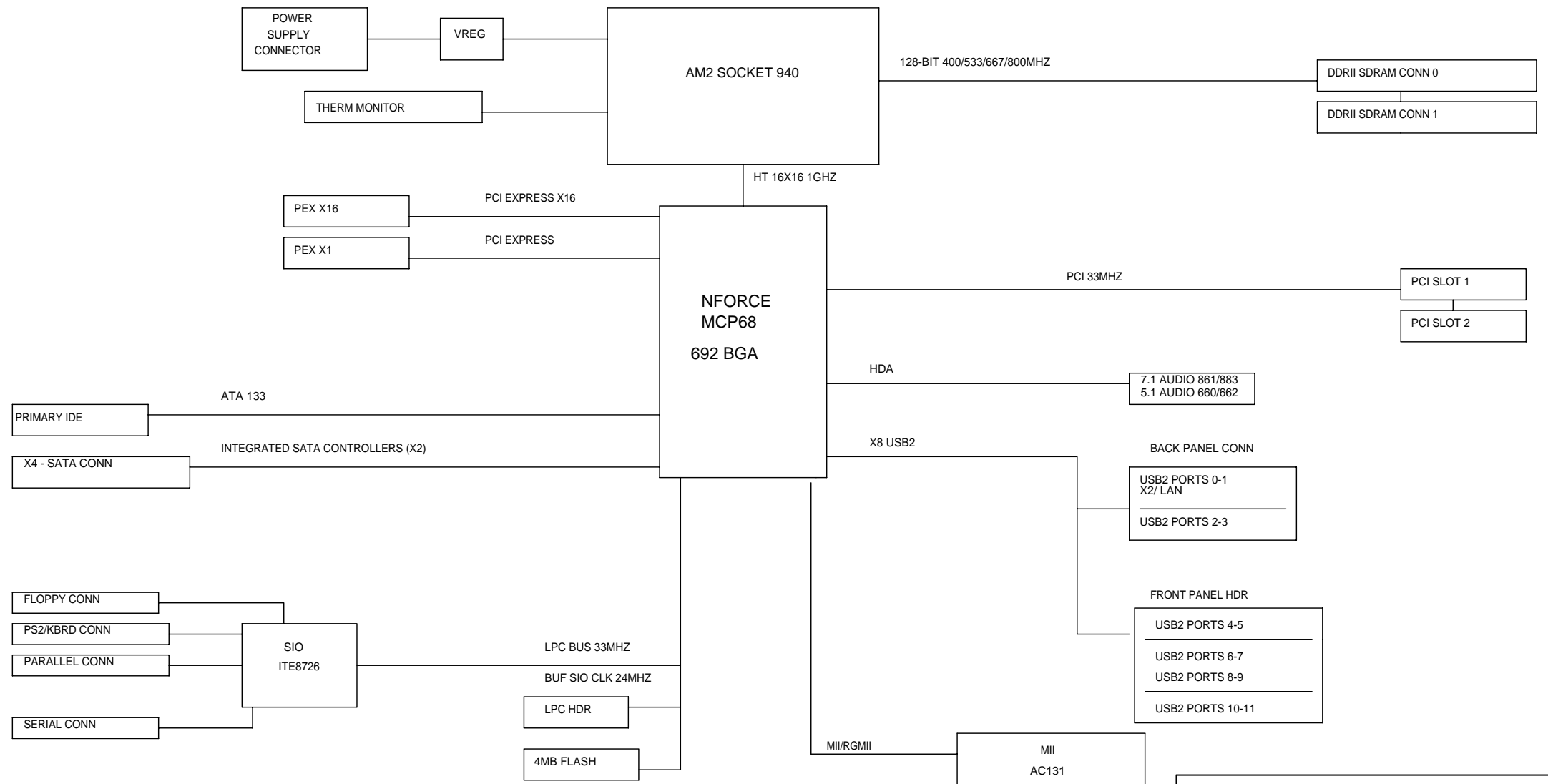
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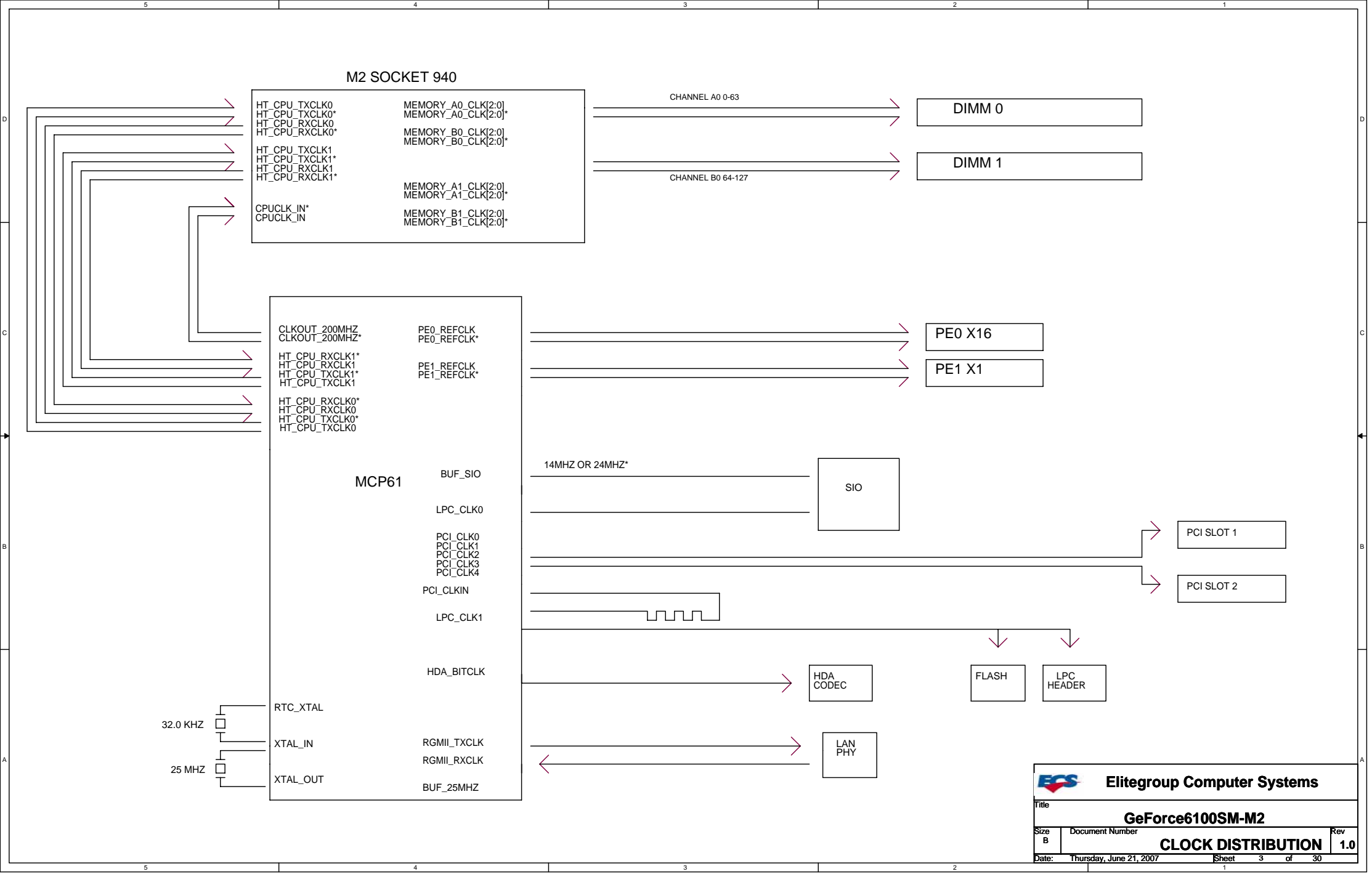
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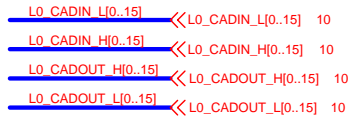
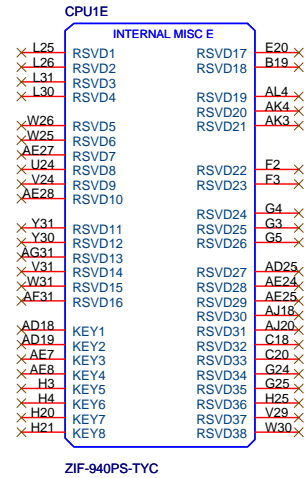
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<i>Layout</i>	Susan/Angela	05/29/2007
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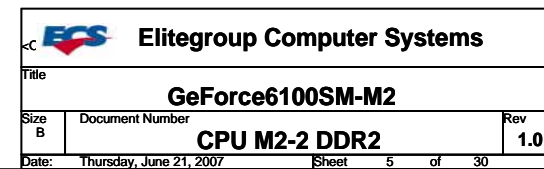
 Elitegroup Computer Systems		
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GeForce6100SM-M2		
Size	Document Number	Rev
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COVER PAGE		
Date:	Thursday, June 21, 2007	Sheet 1 of 30

BLOCK DIAGRAM

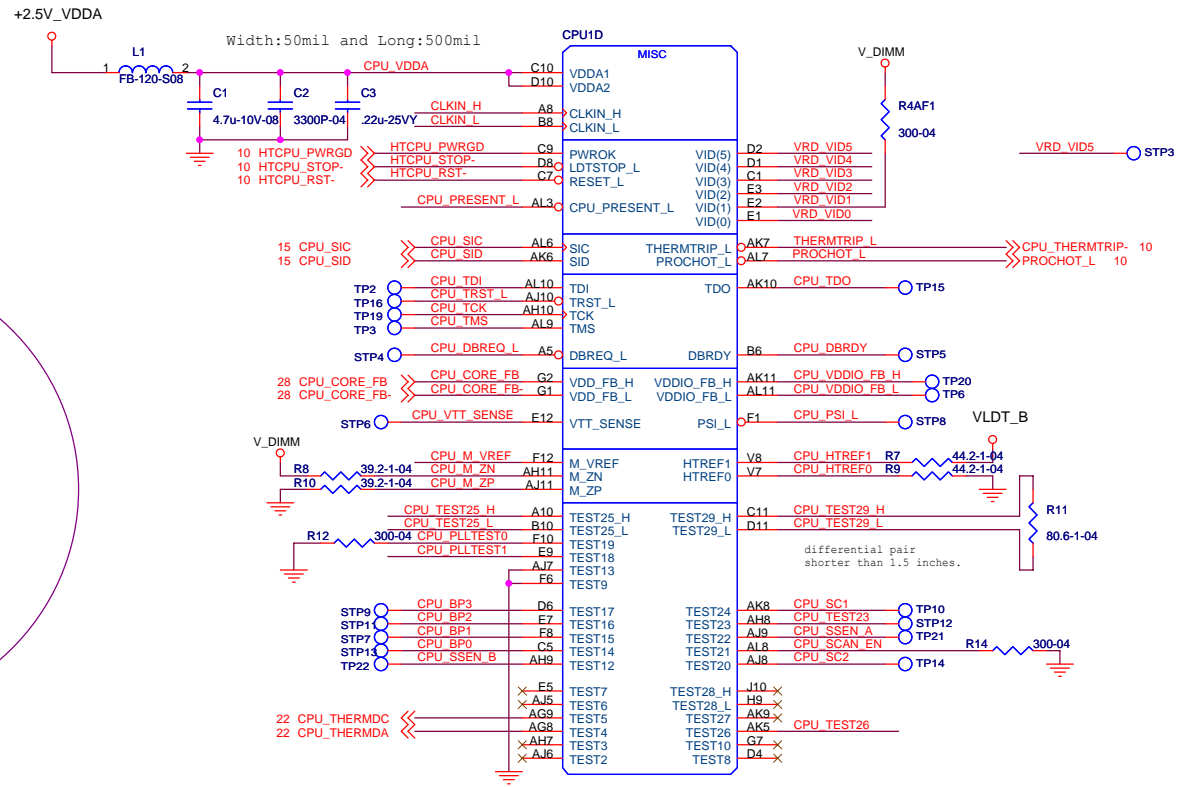
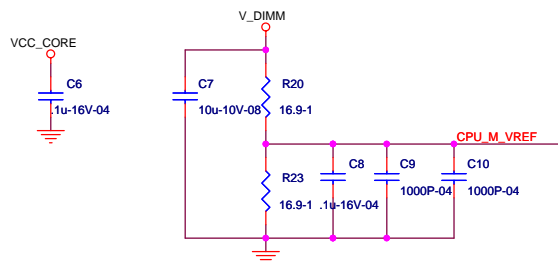
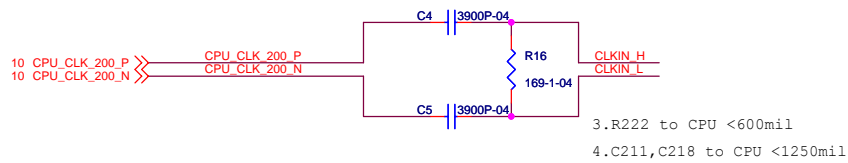
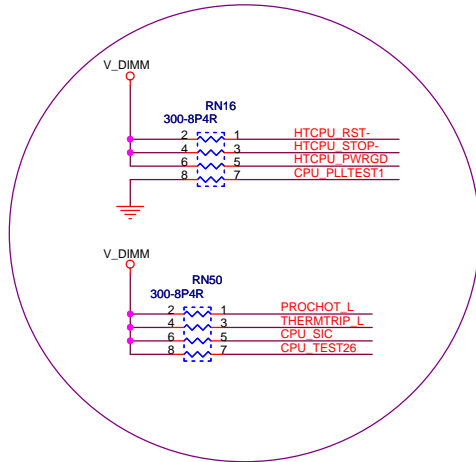
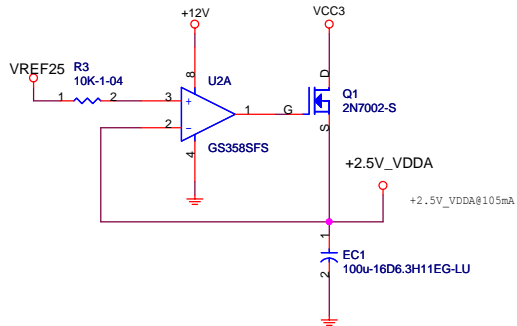




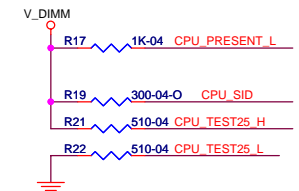


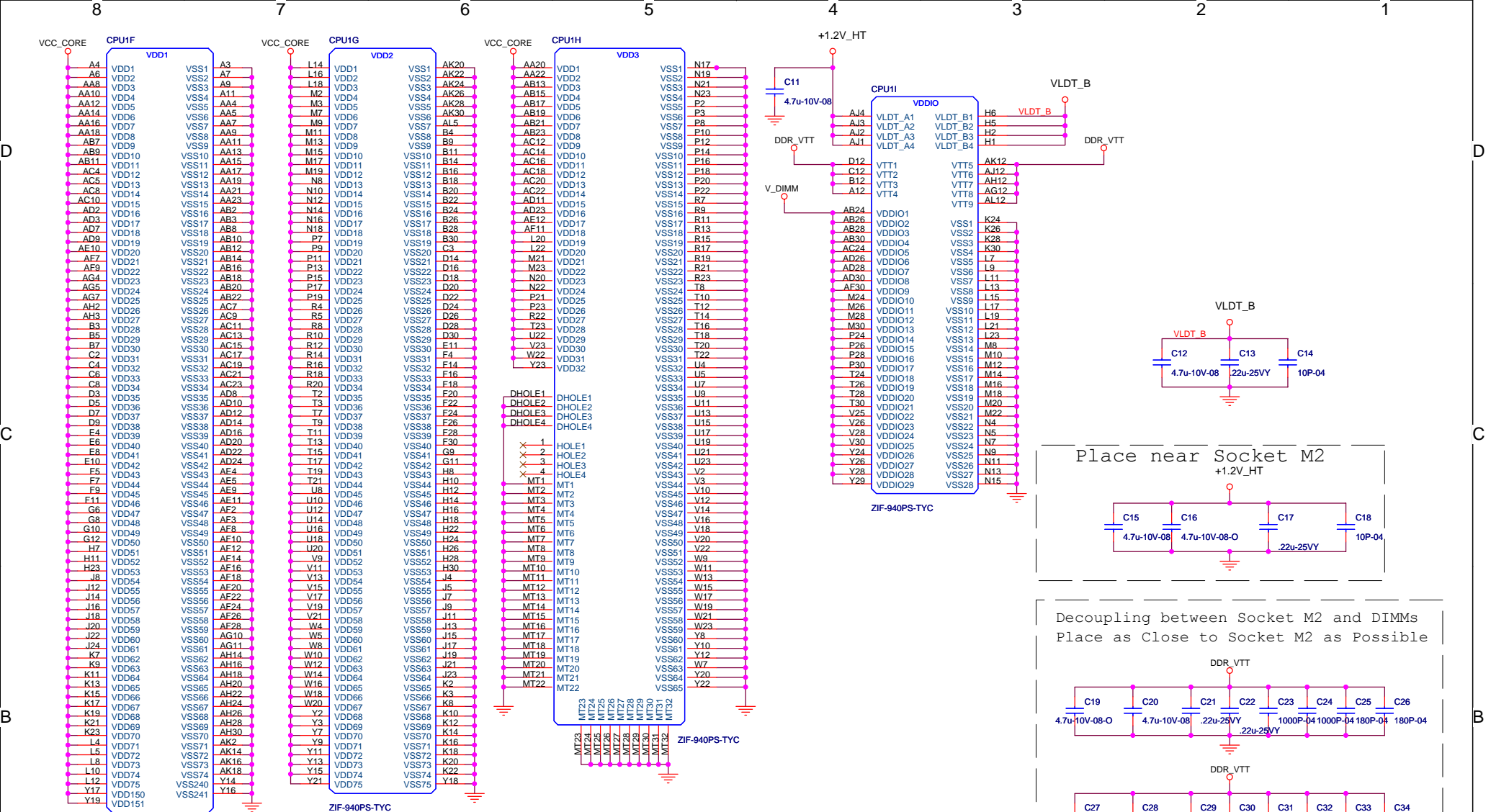


+2.5V_VDDA for CPU PLL



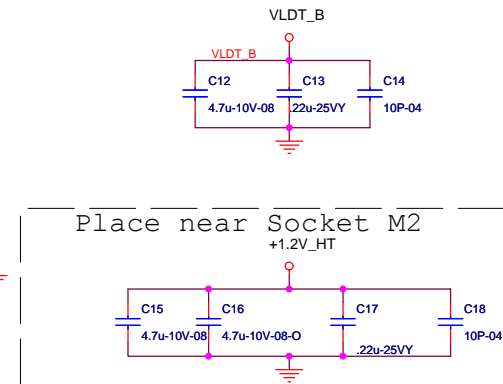
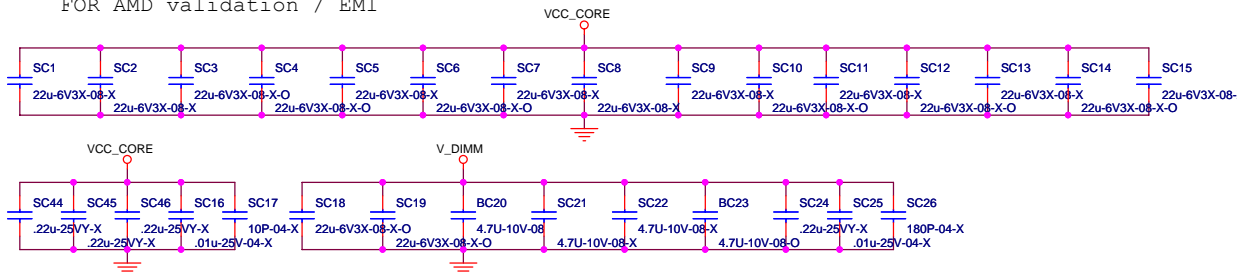
ZIF-940PS-TYC



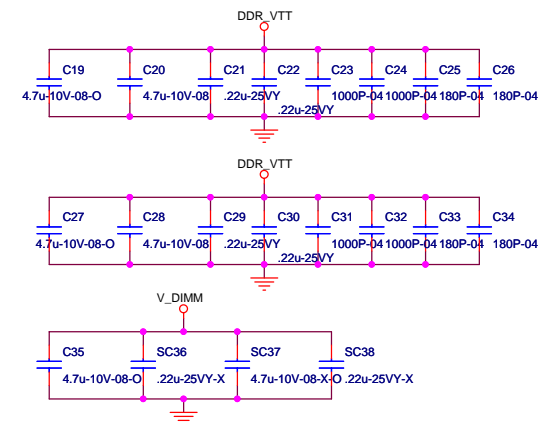


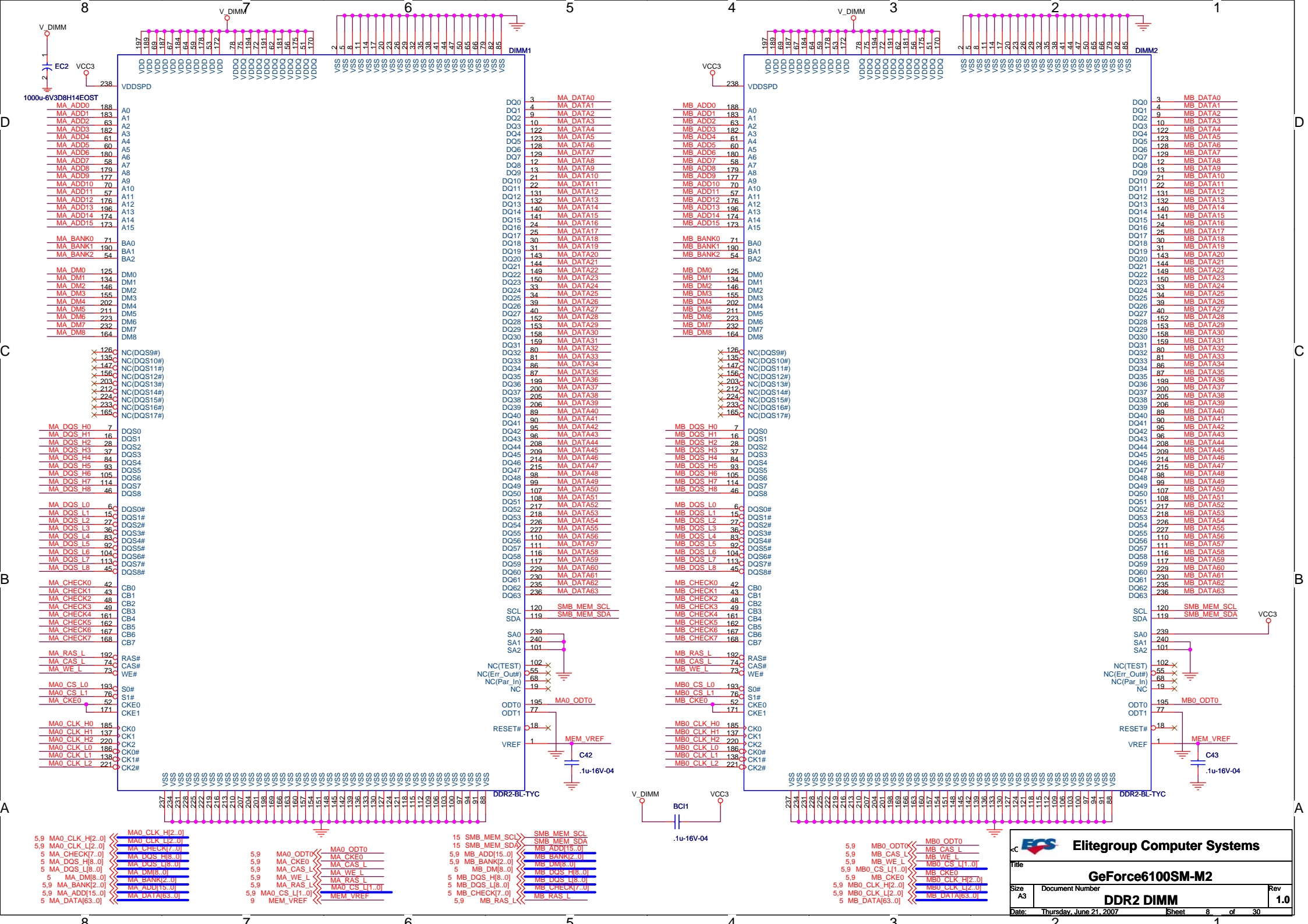
Place Decoupling Capacitors on Bottom Side underneath Socket M2

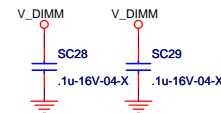
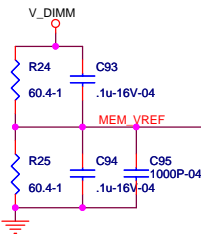
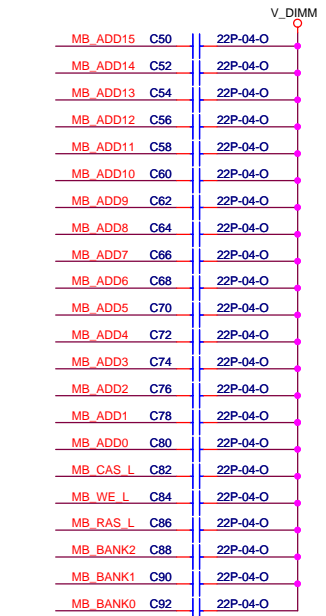
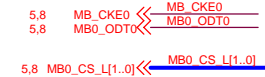
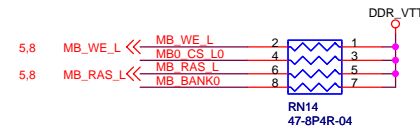
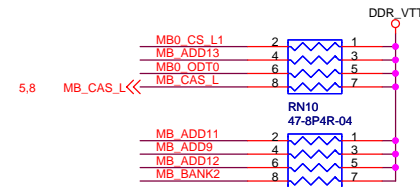
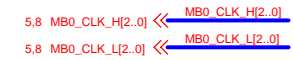
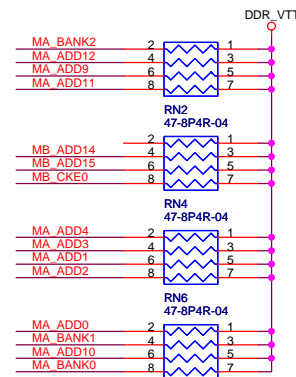
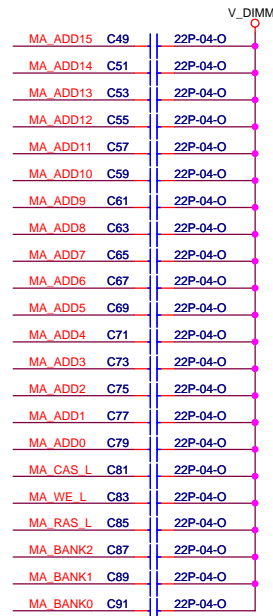
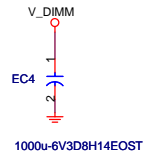
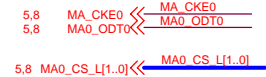
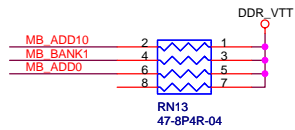
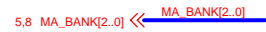
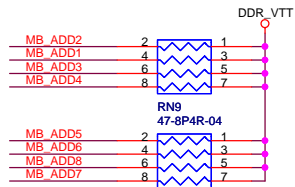
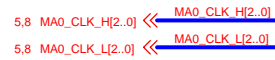
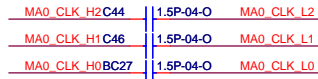
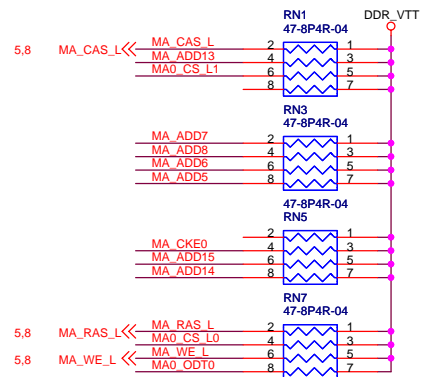
FOR AMD validation / EMI



Decoupling between Socket M2 and DIMMs
Place as Close to Socket M2 as Possible

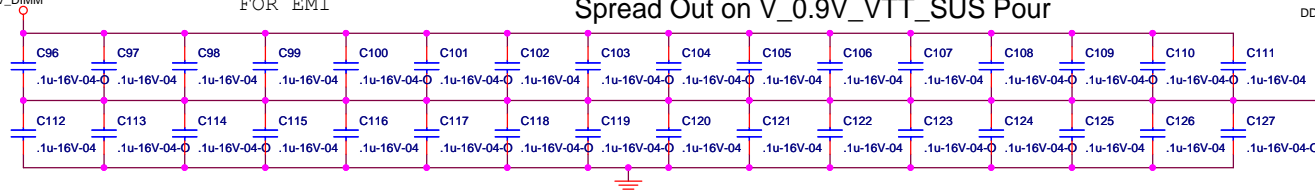


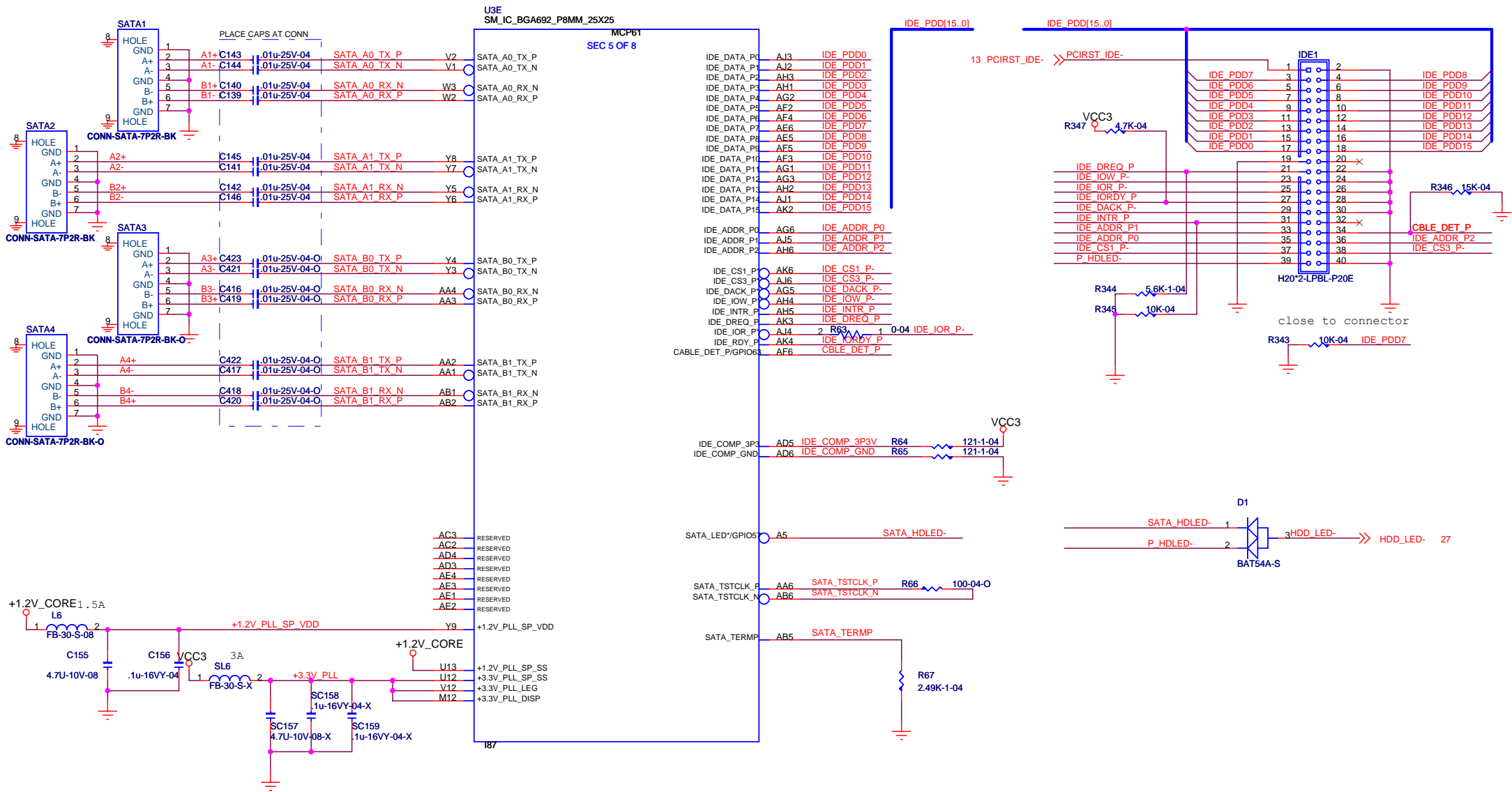




FOR EMI

Spread Out on V_0.9V_VTT_SUS Pour

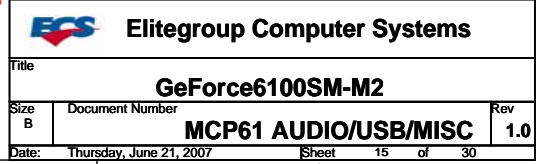




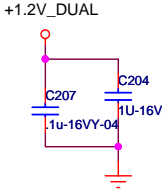
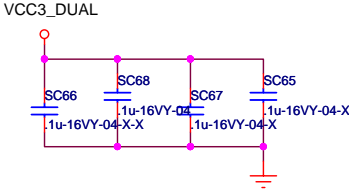
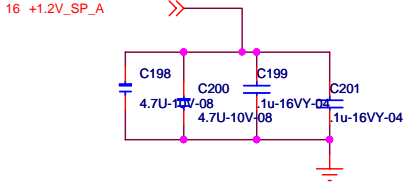
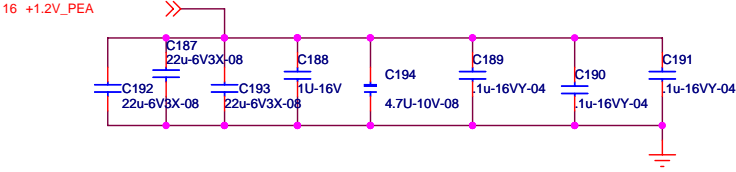
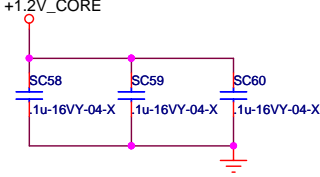
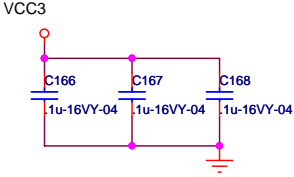
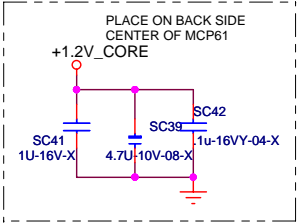
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USB0~3 --> BACK CONNECTORS
USB4~11 --> ON-BOARD HEADER

```



MCP61/8 DECOUPLING/EMI



MCP61 INTERNAL PULL-UP/DWN'S

PE0_PRSNTX16* PE0_PRSNTX8*	10K PU TO 3.3V 10K PU TO 3.3V
PE1_PRSNT* PE2_PRSNT*	10K PU TO 3.3V 10K PU TO 3.3V
PE1_CLKREQ*	10K PU TO 3.3V
PCI_PME*/GPIO_30	8.2K PU TO 3.3V_DUAL
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3 LPC_DRQ1/LPC_CS* LPC_DRQ0* LPC_SERIRQ	8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 10K PU TO 3.3V
HDA_SDATA_IN1/GPIO_23/MGPIO_0 HDA_SDATA_IN0/GPIO_22	10K PD TO GND 10K PD TO GND
JTAG_TMS JTAG_TRST* JTAG_TDI	10K PU TO 3.3V 10K PD TO GND 10K PU TO 3.3V
A20GATE PE_WAKE* EXT_SMI*/GPIO32 THERM*/GPIO_59 KBRDRSTIN*/GPIO_58 R1*/GPIO_33 SIO_PME*/GPIO_31/MGPIO_2 PWRBTN* RSTBTN*	10K PU TO 3.3V 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V 10K PU TO 3.3V 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL

MCP61 SPI CLK STRAP

SPI_DO | SPI_CLK

00 = 500KHZ
01 = 1.8MHZ
10 = 2.5MHZ
11 = 25MHZ


*DEFAULT

MCP68 SPI CLK STRAP

SPI_DO | SPI_CLK

00 = 31MHZ
01 = 42MHZ
10 = 25MHZ
11 = 1MHZ

*DEFAULT

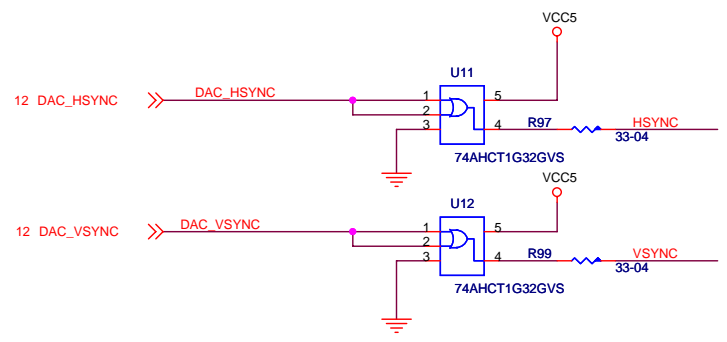
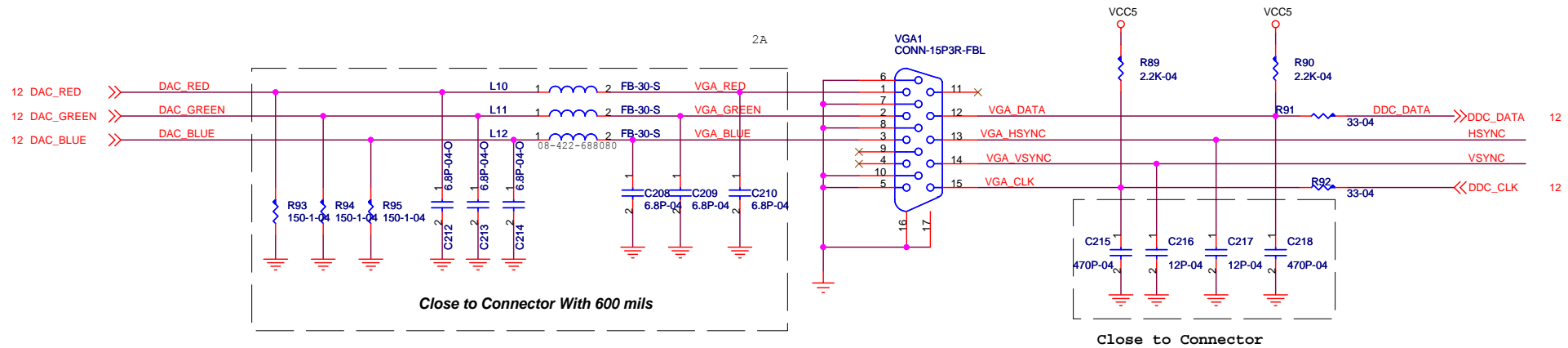
**Elitegroup Computer Systems**

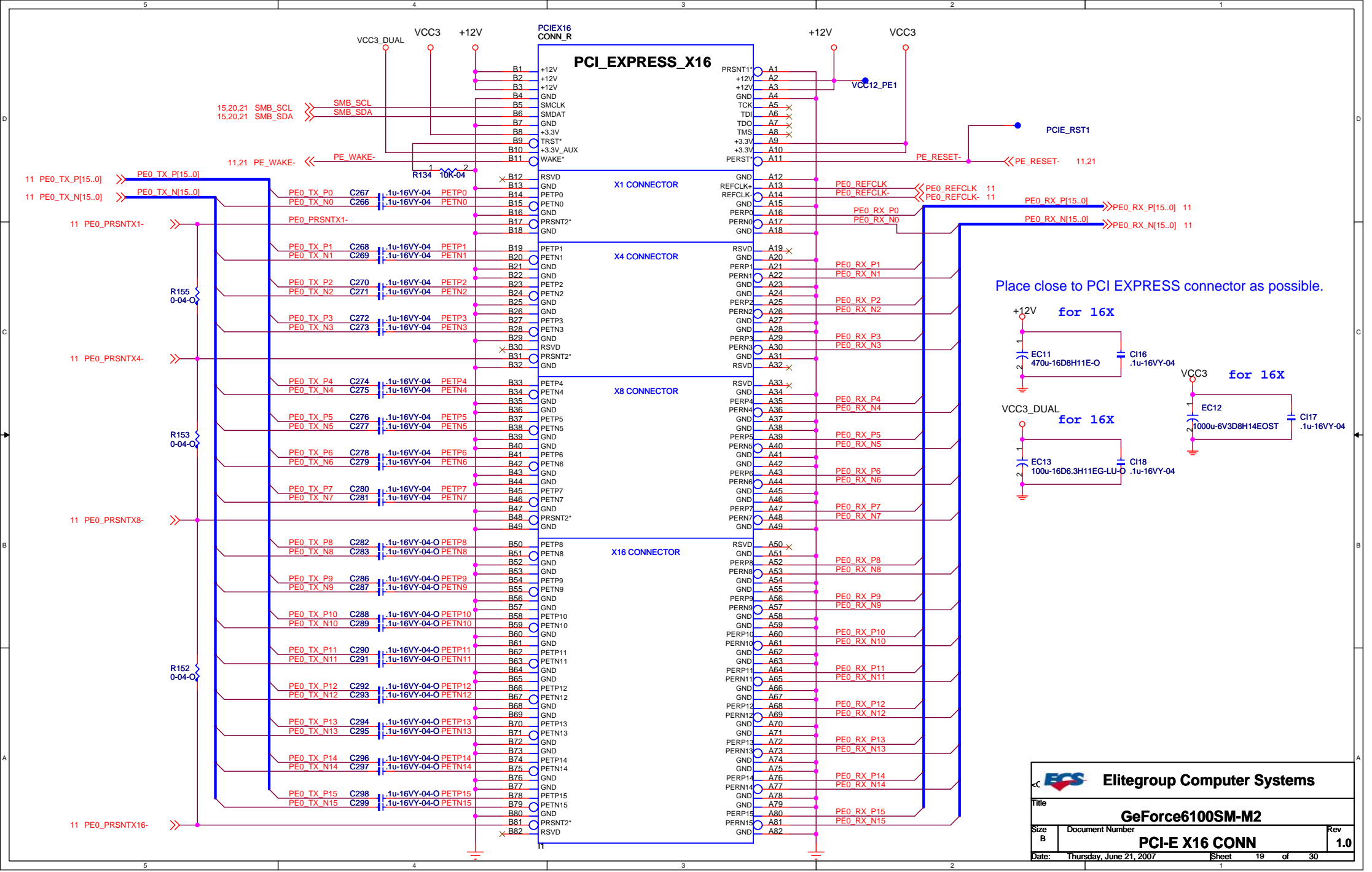
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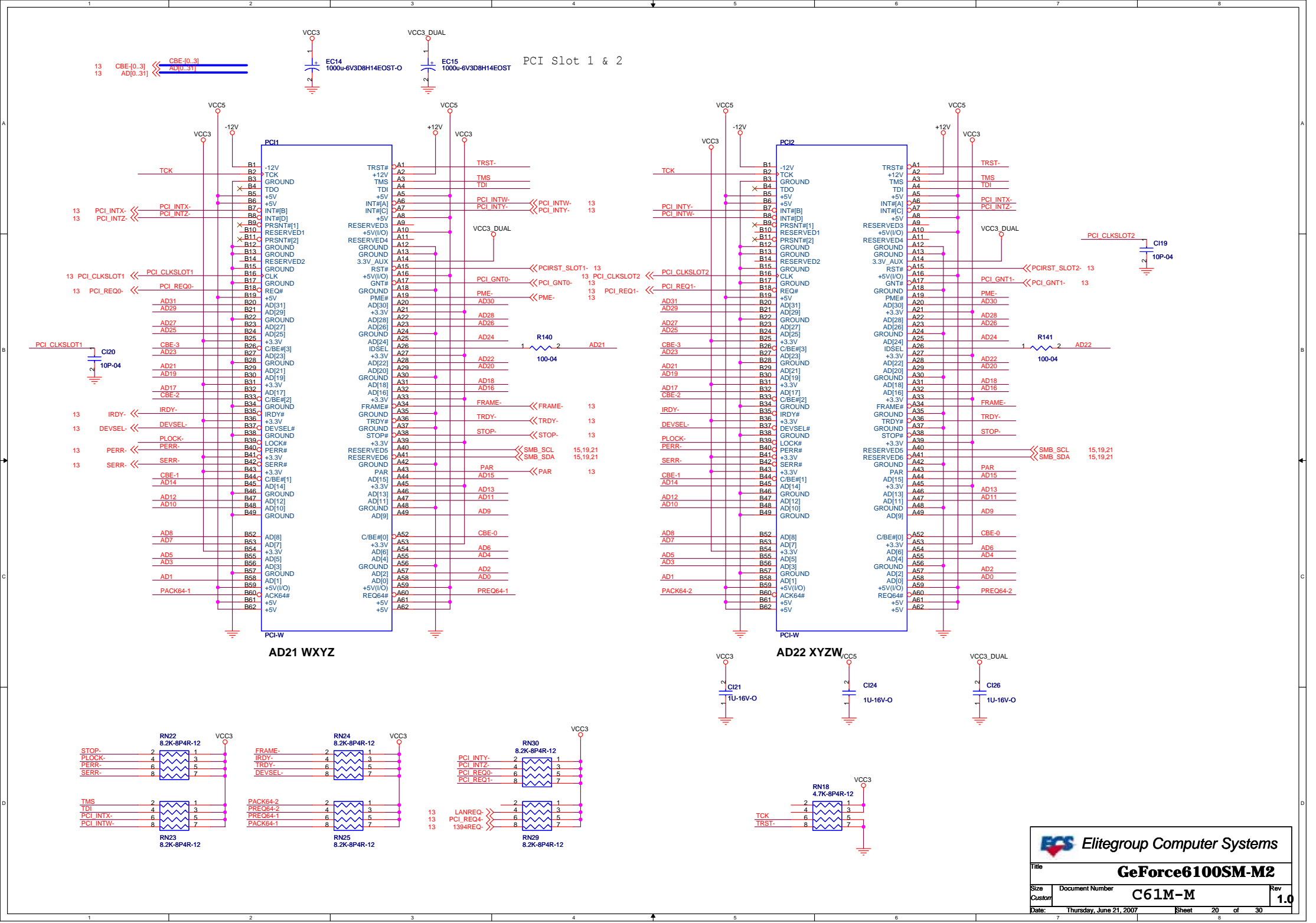
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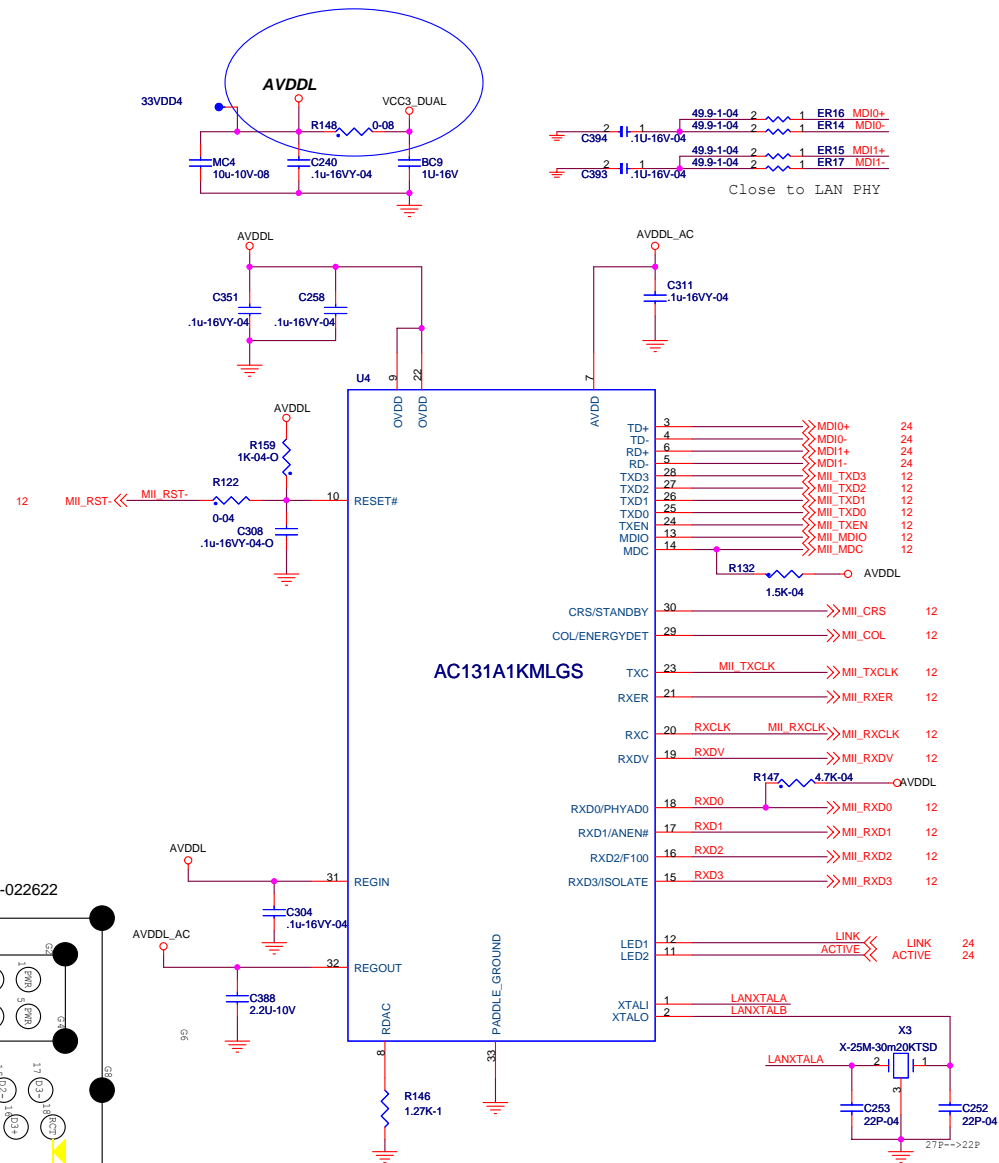
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Date: Thursday, June 21, 2007Sheet 17 of 30



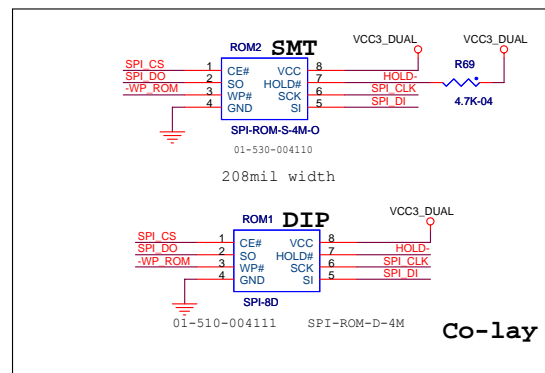




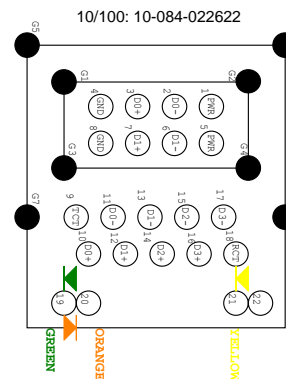


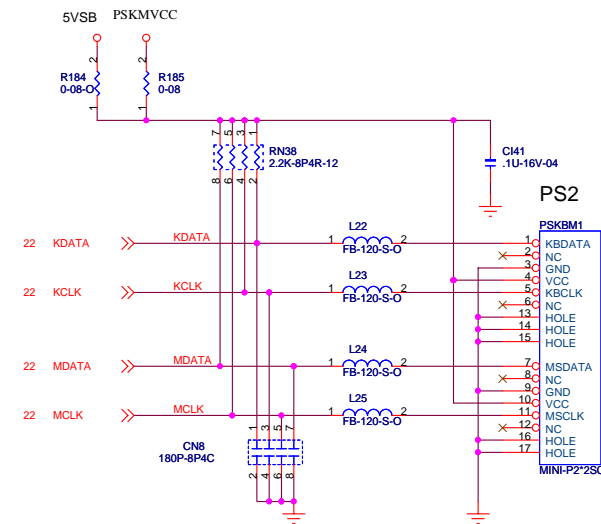
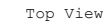
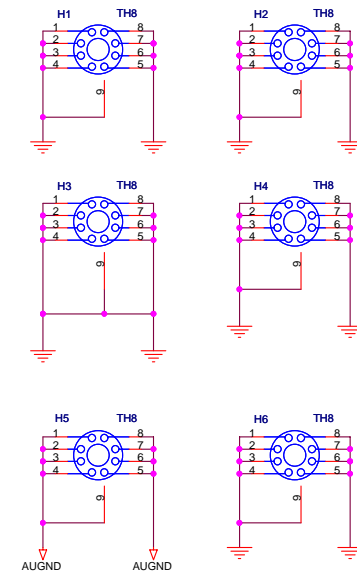
A diagram of a connector with a 150 mil pitch. It shows a central rectangular area labeled "150 mil" with four pins on each side, totaling eight pins. This central area is flanked by two larger rectangular areas, each with four pins on its outer edge, totaling eight pins on each side. The entire assembly consists of 24 pins in total.

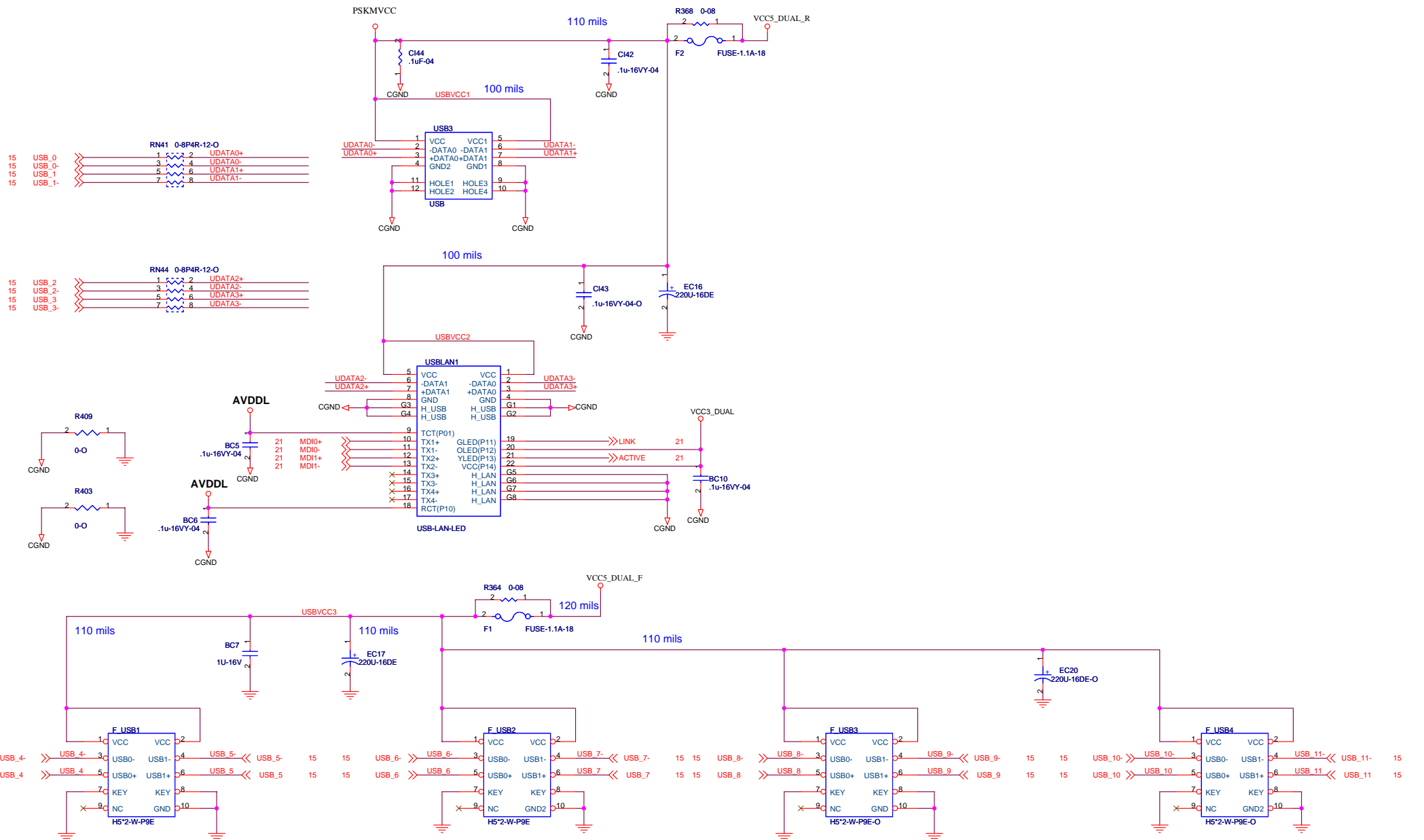
208 mil



for SPI ROM







The schematic diagram illustrates the audio input section of the ADXL345 evaluation board. It is organized into three main functional blocks: Line in, Front out, and Mic in.

- Line in:** This section includes inputs SW_C, PORT-C_L, and PORT-C_R. It features feedback components FB3, FB4, and C335, C336, which are connected to AUGND. The output is connected to the Line in pins (G3, G4, G5, G6).
- Front out:** This section includes outputs SW_D, PORT-D_L, and PORT-D_R. It features feedback components FB5, FB6, and C341, C342, which are connected to AUGND. The output is connected to the Front out pins (E3, E4, E5).
- Mic in:** This section includes inputs SW_B, PORT-B_L, and PORT-B_R. It features feedback components FB7, FB8, and C343, C344, which are connected to AUGND. The output is connected to the Mic in pins (F3, F4, F5).

Additional components shown include MIC-VREF_R and MIC-VREF_L, and various ground connections (AUGND). The diagram is dated 2004/07/01.

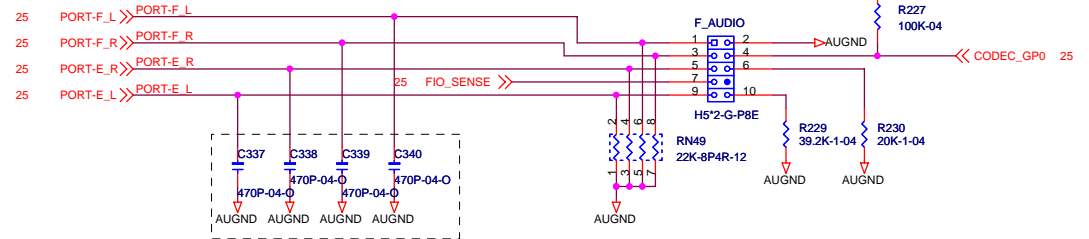
Center/Bass out

Surround

Side-Surround

* Implement Block G only if PORT-G is configured as I/O port

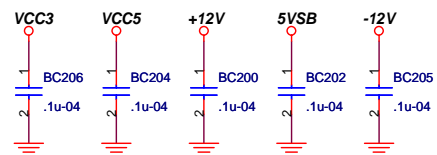
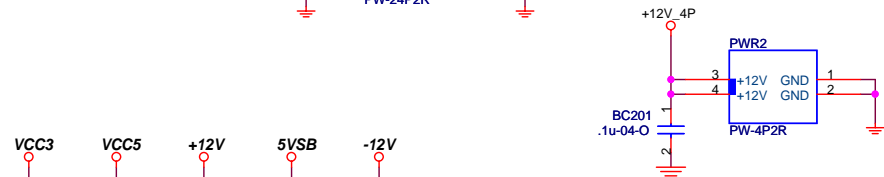
* Implement Block H only if PORT-H is configured as I/O port



TOP VIEW

Diagram showing the top view of a 16-pin DIP package. The pins are numbered 1 through 16. The package is labeled with H1, H2, H3, H4, and H5. The pins are arranged in two rows of 8 pins each. The top row of pins is labeled C2, C3, G1, C4, C5, F2, F3, G2, F4, F5. The bottom row of pins is labeled B2, B3, B4, B5, E2, E3, E4, E5. The pins are also labeled with A2, A3, A4, A5, D2, D3, D4, D5. The package is shown with a central notch and a small square cutout on the right side.





Bypass capacitors close to ATX power connector for EMI solution.

